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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,717	08/26/2003	Kelvin Ma	6198.8-1	4062

23559 7590 04/07/2005

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EXAMINER	
KIANNI, KAVEH C	

ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,717	MA ET AL.	
	Examiner	Art Unit	
	Kianni C. Kaveh	2833	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *1-22,35 and 36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's election without traverse of claims 23-34 in the paper submitted on 1/11/05 is acknowledged. The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 23-28 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wasserbauer (US 2004/0105476).

Regarding claim 23, Wasserbauer teaches an optical integrated circuit (shown in at least figure 1 and 27), comprising: a first optical waveguide 106a formed in a first dielectric layer operable to conduct optical signals (wherein all waveguide and/or optical

interconnect layer is composed of dielectric material, see at least parag. 0081-0082); an optical interconnect 209 formed in a second dielectric layer disposed above the first dielectric layer (see fig. 27, item 209); and a second optical waveguide 160b formed in a third dielectric layer disposed above the second dielectric layer and operable to conduct optical signal whereby the optical interconnect 2092 is operable to conduct optical signals $\lambda 1 \ldots \lambda n$ from the first optical waveguide 106 to the second optical waveguide 104 (see at least parag. 0119).

However, in above Wasserbauer does not specifically teach wherein the above optical signal conducted by the second waveguide is optical signals. This limitation is more specifically taught by Little in another embodiment(see at least figure 40, item waveguide(s)). Thus, it would have been obvious to those of ordinary skill in the art when the invention was made to modify/combine different embodiments of Wasserbauer's teaching in order to produce an optical waveguide renounce structure that includes the above limitations since these embodiments are compatible with each other and since such configuration would provide an optical resonance structure in which the layers each can therefore be optimized independently thus providing performance advantage in power and reliability (see parag. 0010).

Regarding claims 24-28 and 32-34, Wasserbauer further teaches wherein the optical interconnect has a disk configuration (see fig. 27, item 302); wherein the optical interconnect has a ring configuration (see fig. 27, item 302); wherein the first optical waveguide and the second optical waveguide are oriented at a predetermined angle

with one another (shown in at least fig. 27 and/or 40, items waveguides); wherein the first optical waveguide and the second optical waveguide are generally parallel with one another (shown in at least fig.27, items waveguides); wherein the first optical waveguide and the second optical waveguide are generally perpendicular to one another (shown in at least fig. 40, items perpendicular waveguides); a conductive contact disposed above the second optical waveguide, the conductive contact operable to make optoelectronic contact with the second optical waveguide (see at least parag. 0104 and 0107); a second conductive contact disposed below the first optical waveguide, the conductive contact operable to make optoelectronic contact with the first optical waveguide (see at least parag. 0104 and 0107); a first circuit component disposed above the second optical waveguide and electrically coupled to the conductive contact; and a second circuit component disposed below the second optical waveguide and electrically coupled to the second conductive contact (see at least parag. 0104 and 0107).

Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wasserbauer as applied to claims 23-28 above, and further in view of Painter et al. (US 2002/0122615).

Regarding claims 29-31, Wasserbauer teach, as stated above, all limitations that claims 29-31 depend on. However, Wasserbauer does not specifically teach wherein the first/second waveguide and optical interconnect comprises a dopant region formed, respectively, in the first/second/third dielectric layer. Nevertheless, Wasserbauer states

that optical confinement in all dielectric devices/layers are implemented such as with ion implantation and/or oxidation (see at least parag. 0131-0145). This limitation more explicitly taught by Painter et al. (painter) (see at least parag. 0197 and 0224). Thus, it would have been obvious to a person of ordinary skill in the art when the invention was made to modify Wasserbauer interconnect circuit dielectric layers using either, or combinational, teachings of Wasserbauer and/or Painter to dope the above dielectric layers since such doping is conventional and because such configuration would provide an optical resonance structure in which the ring and waveguides lie in different layers and each can therefore be optimized independently thus providing performance advantage in power and reliability (see parag. 0010).

Claim 23--28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Little et al. (Little) (US (6411752).

Regarding claim 23, Little et al. (Little) teaches an optical integrated circuit (shown in at least figure 1), comprising: a first optical waveguide 106 formed in a first dielectric layer operable to conduct optical signals (wherein all waveguide and/or optical interconnect layer is composed of dielectric material, see at least col. 3, 4th parag. And col. 2, and parag.; wherein Si/glass are also dielectric material(s)); an optical interconnect 102 formed in a second dielectric layer disposed above the first dielectric layer; and a second optical waveguide 104 formed in a third dielectric layer disposed above the second dielectric layer and operable to conduct optical signal whereby the optical

interconnect 102 is operable to conduct optical signals $\lambda 1 \ldots \lambda n$ from the first optical waveguide 106 to the second optical waveguide 104 (see at least col. 1, 5th parag.).

However, in above embodiment Little does not specifically teach wherein the above optical signal conducted by the second waveguide 104 is optical signals. This limitation is more specifically taught by Little in another embodiment(see figure 9, item 906). Thus, it would have been obvious to those of ordinary skill in the art when the invention was made to modify/combine different embodiments of Little's teaching in order to produce an optical waveguide renounce structure that includes the above limitations since these embodiments are compatible with each other and since such configuration would provide an optical resonance structure in which the ring and waveguides lie in different layers and each can therefore be optimized independently (see col. 2, 5th parag.).

Regarding claims 24-28 Little further teaches wherein the optical interconnect has a disk configuration (see fig. 1, item 302); wherein the optical interconnect has a ring configuration (see fig. 1, item 302); wherein the first optical waveguide and the second optical waveguide are oriented at a predetermined angle with one another (shown in at least fig. 1 and/or 5, items waveguides); wherein the first optical waveguide and the second optical waveguide are generally parallel with one another (shown in at least fig.1, items waveguides); wherein the first optical waveguide and the second optical waveguide are generally perpendicular to one another (shown in at least fig. 5, items waveguides);

Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Little as applied to claims 23-28 above, and further in view of Painter et al. (US 2002/0122615).

Regarding claims 29-31, Little teaches, as stated above, all limitations that claims 29-31 depend on. However, Little does not explicitly teach wherein the first/second waveguide and optical interconnect comprises a dopant region formed, respectively, in the first/second/third dielectric layer. This limitation more is taught by Painter et al. (painter) (see at least parag. 0197 and 0224). Thus, it would have been obvious to a person of ordinary skill in the art when the invention was made to modify Little et al.'s interconnect circuit dielectric layers using teachings of Wasserbauer in order to dope the above dielectric layers since such doping is conventional and because such configuration would provide an optical resonance structure can therefore be optimized independently thus providing performance advantage in power and reliability (see parag. 0010).

Citation of Relevant Prior Art

Prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In accordance with MPEP 707.05 the following references are pertinent in rejection of this application since they provide substantially the same information disclosure as this patent does. These references are:

Painter t al. 6839491

Ksendzov et al. 6690687

Kolodziejski et al. 2003/0128922

Griffle et al. 20020154674

These references are cited herein to show the relevance of the apparatus/methods taught within these references as prior art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to K. Cyrus Kianni whose telephone number is (571) 272-2417. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 6:00 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font, can be reached at (571) 272-2415.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or:

Hand delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956.

K. Cyrus Kianni
Patent Examiner
Group Art Unit 2883

March 24, 2005